

DATA SHEET

74ALVCH162244

16-bit buffer/line driver
with 30Ω termination resistor (3-State)

Product specification

1998 Jun 29

IC24 Data Handbook

16-bit buffer/line driver with 30Ω termination resistor (3-State)

74ALVCH162244

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on all data inputs
- Integrated 30Ω termination resistor

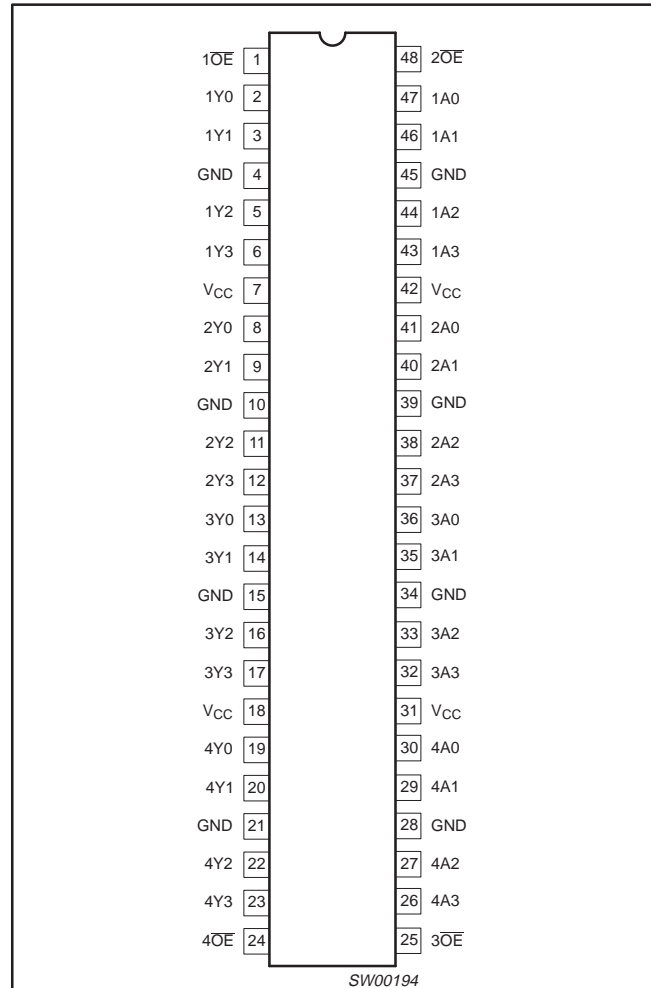
DESCRIPTION

The 74ALVCH162244 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVCH162244 is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The 74ALVCH162244 is designed with 30Ω series resistors in both HIGH and LOW output states.

The 74ALVCH162244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



QUICK REFERENCE DATA

$GND = 0\text{ V}$; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	$V_{CC} = 2.5\text{V}$, $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$	3.0 2.7	ns	
C_I	Input capacitance		5.0	pF	
C_{PD}	Power dissipation capacitance per buffer	$V_I = GND$ to V_{CC}^1	Outputs enabled	25	pF
			Outputs disabled	4	

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to $+85^\circ\text{C}$	74ALVCH162244 DL	ACH162244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to $+85^\circ\text{C}$	74ALVCH162244 DGG	ACH162244 DGG	SOT362-1

16-bit buffer/line driver with 30Ω termination resistor (3-State)

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PIN DESCRIPTION

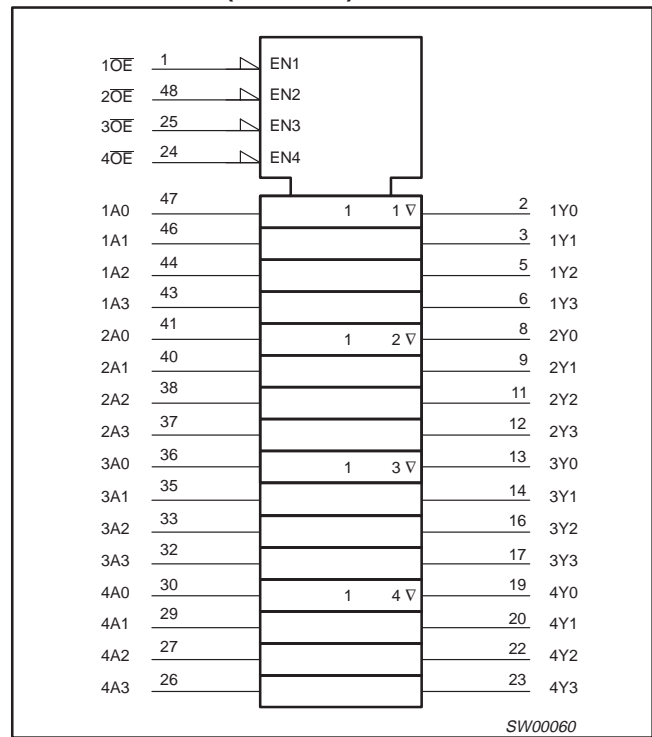
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	
19, 20, 22, 23	4Y0 to 4Y3	
24	4OE	Output enable input (active LOW)
25	3OE	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	
41, 40, 38, 37	2A0 to 2A3	
47, 46, 44, 43	1A0 to 1A3	
48	2OE	Output enable input (active LOW)

FUNCTION TABLE

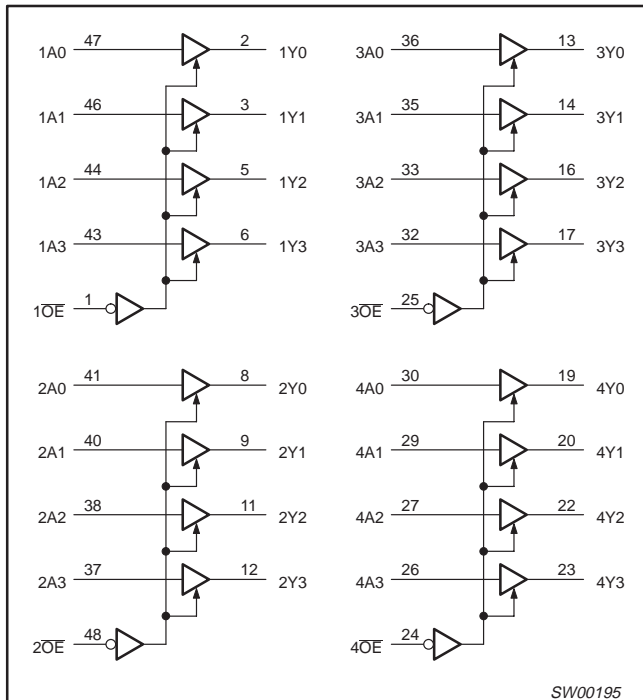
INPUTS		OUTPUT
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

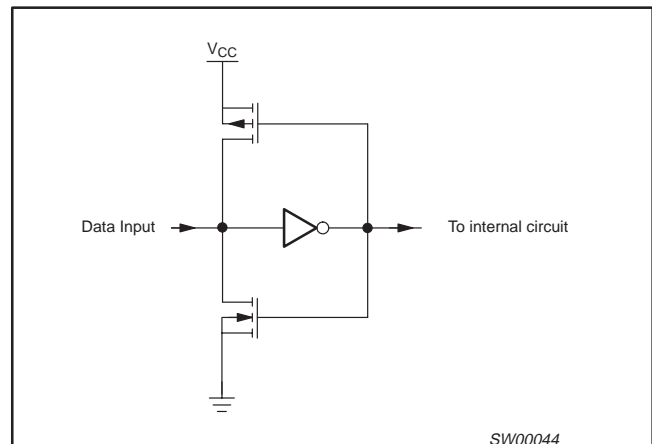
LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



BUS HOLD CIRCUIT



16-bit buffer/line driver with 30Ω termination resistor (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V _I	DC Input voltage range		0	V _{CC}	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 2.3 to 3.0V V _{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage	For data inputs with bus hold ¹	-0.5 to V _{CC} +0.5	V
		For control pins ¹	-0.5 to +4.6	
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0	±50	mA
V _O	DC output voltage	Note 1	-0.5 to V _{CC} +0.5	V
I _O	DC output source or sink current	V _O = 0 to V _{CC}	±50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		±100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	600	

NOTE:

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

16-bit buffer/line driver with 30Ω termination resistor (3-State)

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 2.3 to 2.7V	1.7	1.2		V
		V _{CC} = 2.7 to 3.6V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 2.3 to 2.7V		1.2	0.7	V
		V _{CC} = 2.7 to 3.6V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}		V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -4mA	V _{CC} - 0.4	V _{CC} - 0.11		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} - 0.6	V _{CC} - 0.17		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -4mA	V _{CC} - 0.5	V _{CC} - 0.09		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -8mA	V _{CC} - 0.7	V _{CC} - 0.19		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} - 0.6	V _{CC} - 0.13		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 1.0	V _{CC} - 0.27		
V _{OL}	LOW level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 4mA		0.07	0.40	
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.11	0.55	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 4mA		0.06	0.40	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 8mA		0.13	0.60	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.09	0.55	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.19	0.80	
I _I	Input leakage current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND		0.1	5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	μA
I _{CC}	Quiescent supply current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0		0.2	40	μA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.3V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		150	750	μA
I _{BHL} ²	Bus hold LOW sustaining current	V _{CC} = 2.3V; V _I = 0.7V	45	-		μA
		V _{CC} = 3.0V; V _I = 0.8V	75	150		
I _{BHH} ²	Bus hold HIGH sustaining current	V _{CC} = 2.3V; V _I = 1.7V	-45			μA
		V _{CC} = 3.0V; V _I = 2.0V	-75	-175		
I _{BHLO} ²	Bus hold LOW overdrive current	V _{CC} = 3.6V	500			μA
I _{BHHO} ²	Bus hold HIGH overdrive current	V _{CC} = 3.6V	-500			μA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

16-bit buffer/line driver with 30Ω termination resistor (3-State)

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AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGE AND $V_{CC} < 2.3V$

GND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.3$ to $2.7V$			
			MIN	TYP ¹	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	3.0	4.9	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nYn	2, 3	1.0	4.0	6.8	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nYn	2, 3	1.0	2.3	6.3	ns

NOTES:1. All typical values are measured at $T_{amb} = 25^\circ C$ and $V_{CC} = 2.5V$.

AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3 \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.7	4.2	1.0	3.3	4.7	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nYn	2, 3	1.0	3.5	5.6	1.0	4.6	6.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nYn	2, 3	1.0	2.9	5.5	1.0	3.2	5.7	ns

NOTES:1. All typical values are measured at $T_{amb} = 25^\circ C$.2. Typical value is measured at $V_{CC} = 3.3V$

16-bit buffer/line driver with 30Ω termination resistor (3-State)

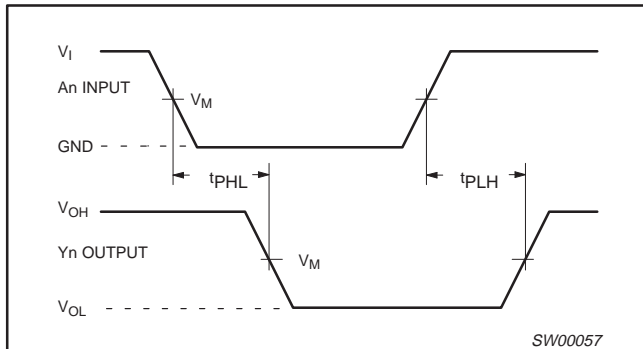
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AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$ AND $V_{CC} < 2.3V$ RANGE

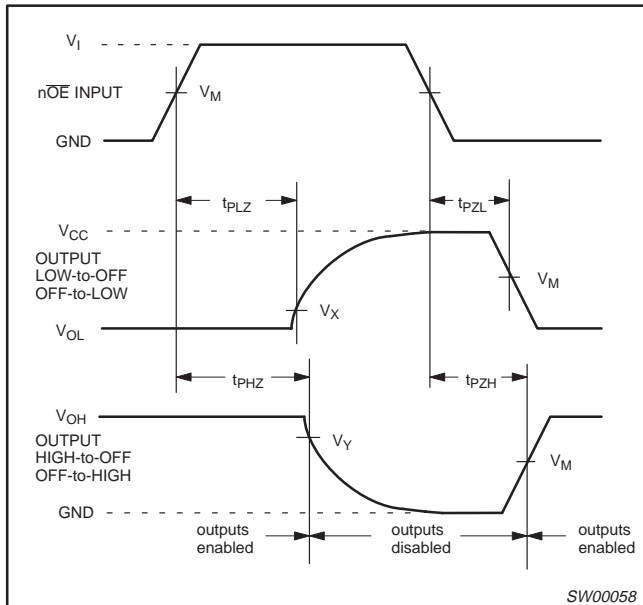
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.15V$
 $V_Y = V_{OH} - 0.15V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$

AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

$V_M = 1.5 V$
 $V_X = V_{OL} + 0.3V$
 $V_Y = V_{OH} - 0.3V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = 2.7V$

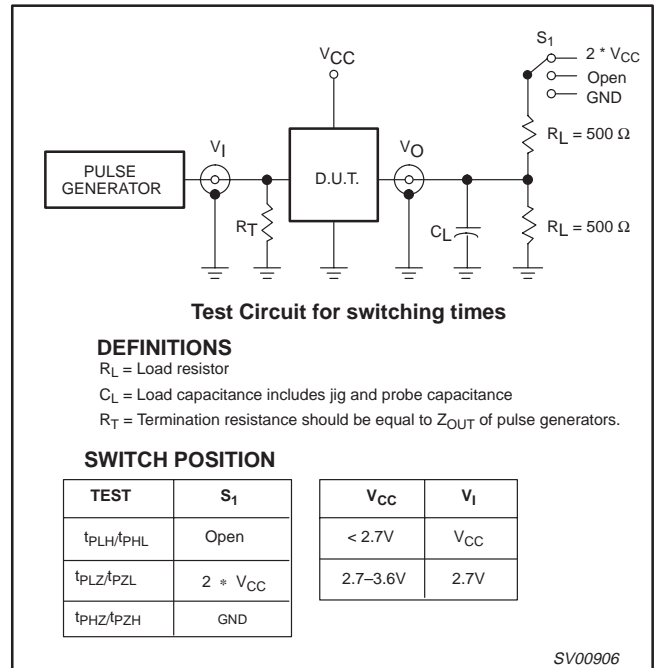


Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



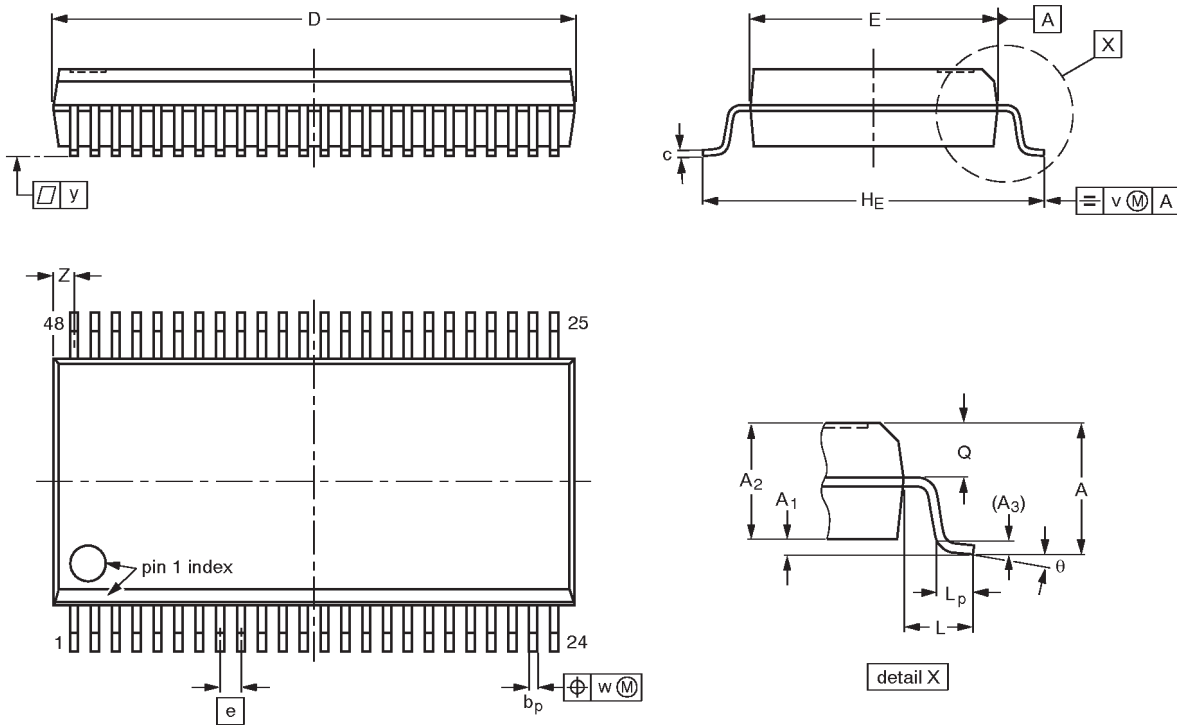
Waveform 3. Load circuitry for switching times

16-bit buffer/line driver with 30Ω termination resistor
(3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

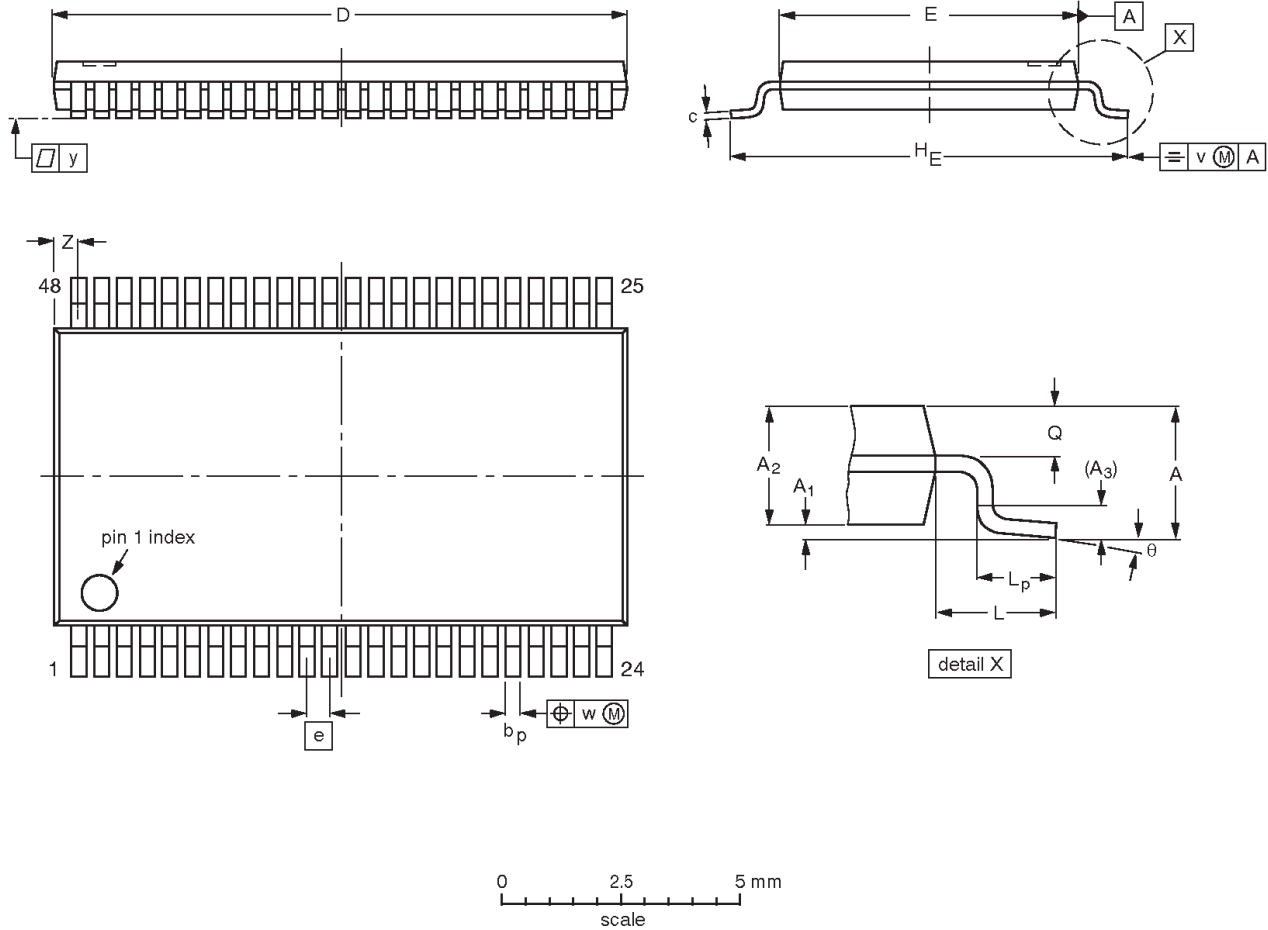
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

16-bit buffer/line driver with 30Ω termination resistor
(3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153ED				93-02-03 95-02-10

16-bit buffer/line driver with 30Ω termination resistor
(3-State)

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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